DC to 500 MHz, Dual Digital Gain Trim Amplifier

Preliminary Technical Data

AD8366

FEATURES

Matched Pair of Differential Digitally-Controlled VGAs
Gain Range: 4.5 dB to 20.5 dB
Step 0.25 dB
Operating frequency
DC to 500MHz
800MHz 3-dB bandwidth
NF 10.5 dB @ max. gain, 18dB @ min. gain at 10MHz
OIP3 36dBVrms at 10MHz
HD2, HD3 > 88dBc for 2Vpp output at 10MHz at max gain
Differential Input and Output
Adjustable output common-mode
Optional DC output offset correction
Serial/Parallel Port Programmable
Power-down Feature
Single 5V Supply Operation

APPLICATIONS

Baseband I/Q receivers
Diversity receivers
ADC drivers
W-CDMA/CDMA/CDMA2000/GSM
Point-to-(Multi)Point Radio
CATV
Wireless local loop
WiMax

FUNCTIONAL BLOCK DIAGRAM

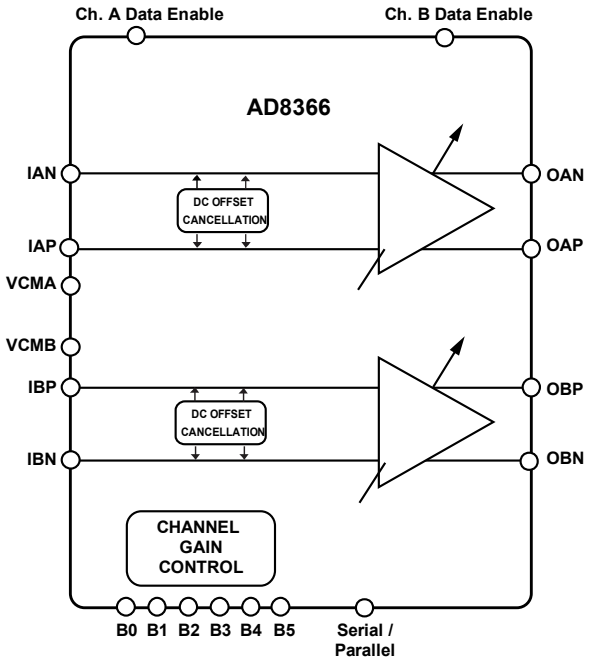

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8366 is a matched pair of fully differential low-noise and low-distortion digitally programmable variable gain amplifiers. The gain of each amplifier can be programmed separately or simultaneously over a range of 5 dB to 21 dB in steps of 0.25 dB. The amplifier offers flat frequency performance and group delay from DC out to 150 MHz, independent of gain code.

The AD8366 offers excellent spurious-free dynamic range, suitable for driving 12-bit ADCs. The NF at max gain is 10.5 dB at 10 MHz and increases 2dB for every 4dB decrease in gain. Over the entire gain range, the HD3 and HD2 are >88dBc for 2 V p-p at the output at 10 MHz into 500 **Ω**. The 2-tone intermodulation distortion of -90dBc into 200 **Ω** translates to an OIP3 of 43 dBm. The differential input impedance is 200 **Ω** to provide a well-defined termination. The differential output is voltage-mode with a low impedance of 30 **Ω**.

The output common-mode defaults to $V_{ps}/2$ but can be programmed via pins VCMA and VCMB over a range of voltages. The built-in DC-offset compensation loop can be disabled if DC-coupled operation is desired. The high-pass corner is defined by external capacitors on pins OFSA and OFSB. The input common mode also defaults to $V_{ps}/2$ but can be driven from 1.2V to 3.4V.

The digital interface allows for parallel or serial gain programming. The AD8366 operates off a 4.5V to 5.5V supply and consumes a supply current of 175mA. When disabled, it consumes ~ 4mA. The AD8366 is fabricated using Analog Devices' advanced Silicon-Germanium bipolar process and is available in a 32-lead exposed paddle LFCSP package. Performance is specified over a -40°C to +85°C temperature range.

Rev. PrC
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REVISION HISTORY

10/07—Revision PrA: Initial Version

02/08—Revision PrB: Updated Performance Specifications

06/08—Revision PrC: Evaluation Board Section

SPECIFICATIONS

VS. = 5 V, T_A = 25°C, Z_s = 200 Ω, Z_L = 200 Ω, f = 10 MHz, unless otherwise noted

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth	3dB; all gain codes		1000		MHz
	1dB; all gain codes		250		MHz
Slew Rate	Max. Gain		TBD		V/ns
	Min. Gain		TBD		V/ns
INPUT STAGE	IPPA, IPMA, IPPB, IPMB				
Maximum Input Swing	At minimum gain A_v=4.5dB		3.2		Vp-p
Differential Input Impedance			200		Ώ
Input Common Mode Range	1Vp-p Input	TBD		TBD	V
	Input pins left floating		Vps/2		
GAIN					
Voltage Gain Range		4.5		20.5	dB
Gain Step Size	All gain codes		0.25		dB
0.1dB Gain Flatness	Max. Gain		150		MHz
Mismatch	Channels A and B at same gain code		+/- 0.05dB		dB
Group Delay Flatness	All gain codes, 20% frac. bandwidth, fc<100MHz		<0.5		ns
Mismatch	Channels A and B at same gain code		2		ps
Gain Step Response	Max. gain to Min. gain		TBD		ns
	Min. gain to Max gain		TBD		ns
Common-mode Rejection Ratio			TBD		dB
OUTPUT STAGE	OPPA, OPMA, OPPB, OPMB, VCMA, VCMB				
Maximum Output Swing	At maximum gain, A_v=20.5dB		6		Vp-p
Differential Output Impedance			30		Ώ
Output DC offset	Inputs Shorted, offset loop disabled	-15	TBD	-4	mV
Output Common Mode Range	1Vp-p output	1.2		3.4	V
	VCMA and VCMB left floating		Vps/2		V
Common-Mode Setpoint Input Impedance			4		kΩ
NOISE/DISTORTION					
10 MHz					
Noise Figure	Max Gain		10.5		dB
	Min Gain		18		dB
2nd Harmonic	2 Vp-p output, Max Gain, ZL=500Ώ		88		dBc
	2 Vp-p output, Min Gain, ZL=500Ώ		88		dBc
3rd Harmonic	2 Vp-p output, Max Gain, ZL=500Ώ		92		dBc
	2 Vp-p output, Min Gain, ZL=500Ώ		85		dBc
OIP3	2 V p-p composite, Max. Gain, ZL=200Ώ		36		dBVrms
	2 V p-p composite, Min. Gain, ZL= 200Ώ		35		dBVrms
Output 1 dB Compression Point	Max. gain, ZL=500Ώ		7		dBVrms
	Min. Gain, ZL=500Ώ		6.9		dBVrms
50 MHz					
Noise Figure	Max Gain		11.2		dB
	Min Gain		18.5		dB
2nd Harmonic	2 Vp-p output , Max Gain		TBD		dBc
	Min Gain		TBD		dBc
3rd Harmonic	2 V p-p output, Max Gain		TBD		dBc
	Min Gain		TBD		dBc

OIP3	2 V p-p composite, Max. Gain, ZL=500Ω		34.2	dBVrms
	2 V p-p composite, Min. Gain, ZL=500Ω		30.7	dBVrms
Output 1 dB Compression Point	Max. gain, ZL=500Ω		6.7	dBVrms
	Min. Gain, ZL=500Ω		7.2	dBVrms
100 MHz				
Noise Figure	Max Gain		11.84	dB
	Min Gain		18.8	dB
2nd Harmonic	2 Vp-p output , Max Gain		TBD	dBc
	Min Gain		TBD	dBc
3rd Harmonic	2 Vp-p output, Max Gain		TBD	dBc
	Min Gain		TBD	dBc
OIP3	2Vp-p composite, Max. Gain @ 500 Load impedance		29.5	dBVrms
	Min. Gain		21	dBVrms
Output 1 dB Compression Point	Max. gain		4	dBVrms
	Min. Gain		6	dBVrms
DIGITAL LOGIC	SENB, DENA, DENB, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5			
V_{INH}, Input High Voltage		TBD		V
V_{INL}, Input Low Voltage			TBD	V
I_{INH}/I_{INL}, Input Current			TBD	µA
C_{IN}, Input Capacitance			TBD	pF
SPI INTERFACE TIMING	SENB = HIGH			
f_{SCLK}			TBD	MHz
t_1	CS rising edge to first SCLK rising edge	TBD		ns
t_2	SCLK high pulse width	TBD		ns
t_3	SCLK low pulse width	TBD		ns
t_4	SDAT setup time	TBD		ns
t_5	SDAT hold time	TBD		ns
t_6	SCLK falling edge to CS low	TBD		ns
PARALLEL PORT TIMING	SENB = LOW			
t_7	DENA/B high pulse width	TBD		ns
t_8	DENA/B low pulse width	TBD		ns
t_9	BIT[0-5] setup time	TBD		ns
t_{10}	BIT[0-5] hold time	TBD		ns
POWER AND ENABLE	VPSI, VPSO, ICOM, OCOM, ENBL			
Supply Voltage Range		4.5	5.5	V
Total Supply Current	ENBL = 5V		180	mA
Disable Current	ENBL = 0V		3.2	mA
Disable Threshold			TBD	V
Enable Response Time	Delay following high-to-low transition until device meets full specifications		TBD	ns
Disable Response Time	Delay following low-to-high transition until device produces full attenuation		TBD	ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages VPSI, VPSO	5.5 V
ENBL, SENB, DENA, DENB, BIT0, BIT1, BIT2, BIT3, BIT4, BIT5	TBD V
IPPA, IPMA, IPPB, IPMB	TBD V
OPPA, OPMA, OPPB, OPMB	TBD V
OFSA, OFSB	TBD V
DECA, DECB, VCMA, VCMB, CCMA, CCMB	TBD V
Internal Power Dissipation	TBD mW
θ_{JA} (With Pad Soldered to Board)	TBD°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

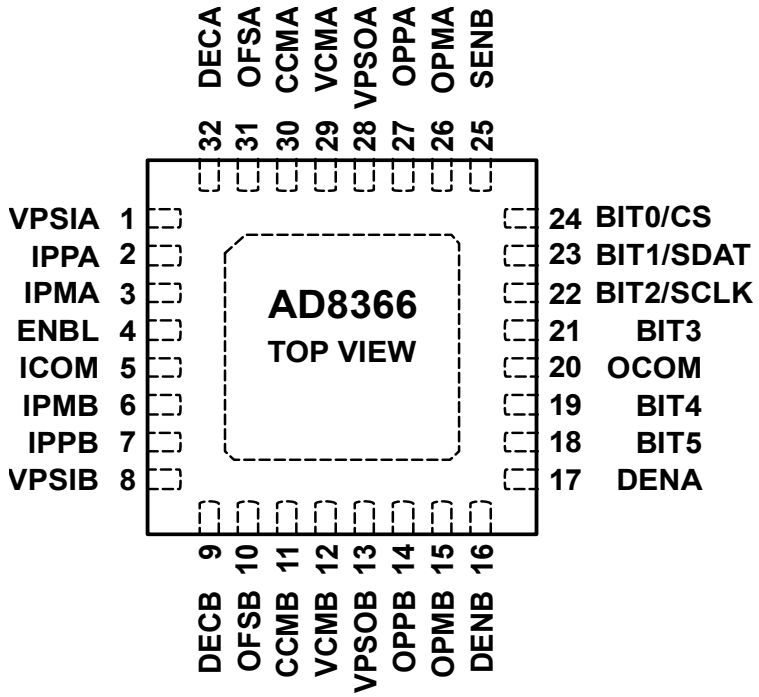

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 13, 28	VPSIA, VPSIB, VPSOA, VPSOB	Input and Output Stage Positive Supply Voltage. 4.5 V – 5.5 V.
2, 3, 6, 7	IPPA, IPMA, IPPB, IPMB	Differential Inputs
4	ENBL	Chip Enable. Pull high to enable.
5, 20	ICOM, OCOM	Input and Output Stage Common. Connect via lowest possible impedance to external circuit common
9, 32	DECA, DECB	Vpos/2 Reference Output Decoupling. Connect decoupling capacitor to circuit common.
10, 31	OFSA, OFSB	Output Offset Correction Loop Compensation. Connect capacitor to circuit common. Tie to common to disable.
11, 30	CCMA, CCMB	Output Common-mode Centering Loop Compensation. Connect capacitor to circuit common
12, 29	VCMB, VCMA	Output Common-mode Setpoint. Defaults to Vpos/2 if left open
14, 15, 26, 27	OPPB, OPMB, OPMA, OPPA	Differential Outputs
16, 17	DENB, DENA	Data enable . Pull high to address each or both channels for parallel load. Not used in serial mode.
18, 19, 21, 22, 23, 24	BIT5, BIT4, BIT3, BIT2, BIT1, BIT0	Parallel data path for SENB pulled low. For SENB pulled high, BIT0 becomes a chip-select (CS), BIT1 becomes serial data input, SDAT, and BIT2 becomes serial clock, SCLK. BIT3-BIT5 are not used in the serial mode
25	SENB	Serial interface enable. Pull high for serial; pull low for parallel.

TYPICAL PERFORMANCE CHARACTERISTICS

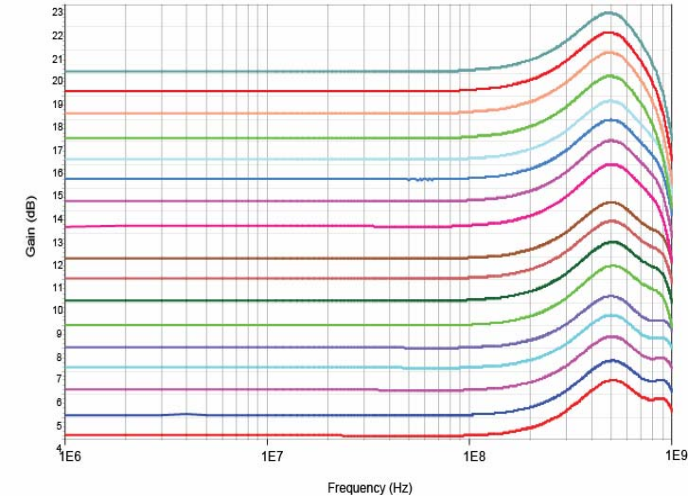

Figure 3. Gain vs. Frequency for Multiple Gain Codes

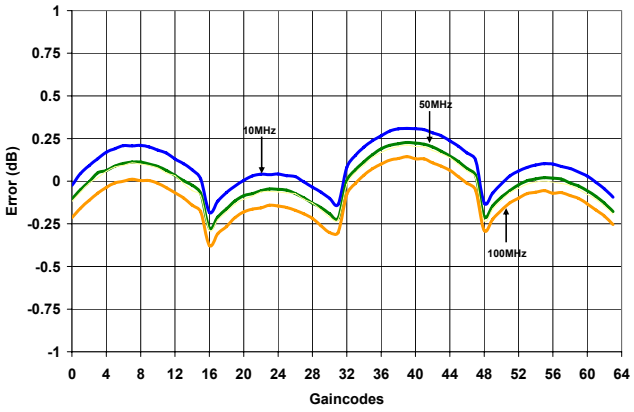

Figure 6. Gain Error vs. Ideal Gain Codes at 10MHz, 50MHz and 100MHz

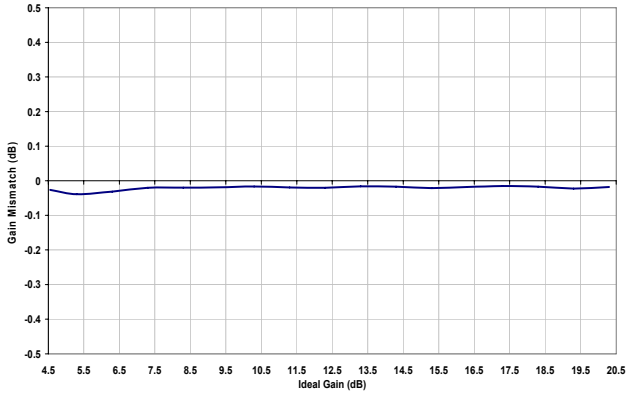

Figure 4. IQ Gain Mismatch at 10 MHz vs. Ideal Gain

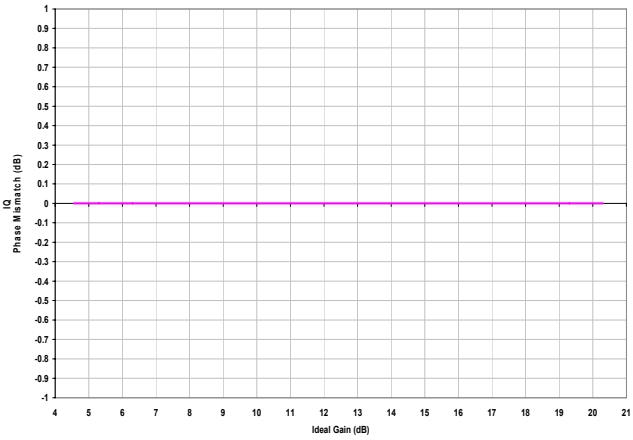

Figure 7. IQ Phase Mismatch at 10 MHz vs. Ideal Gain

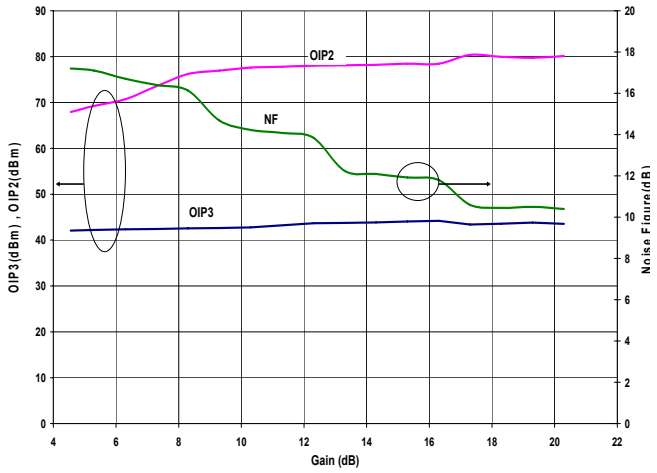

Figure 5.O IP2,OIP3 and NF vs. Gain at 10 MHz

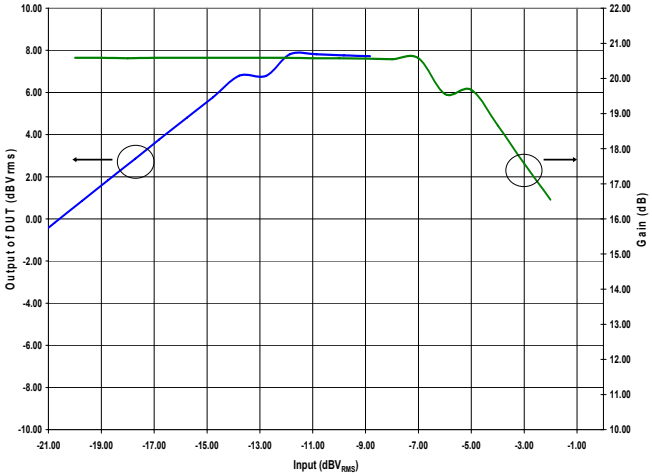

Figure 8. Gain & Output Swing vs. Input Power at Max Gain Setting at 10MHz

APPLICATIONS SCHEMATIC

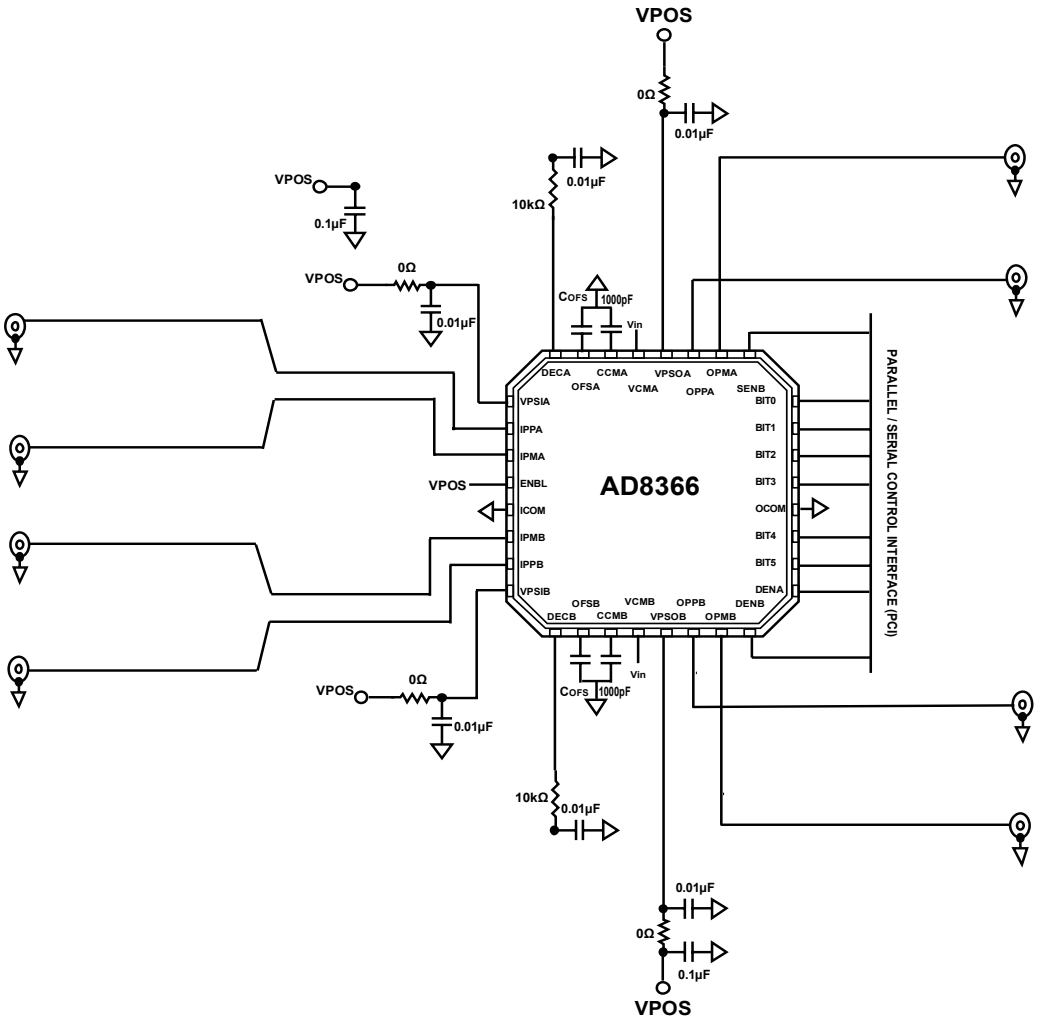

Figure 9 Applications Schematic with Basic Connections

EVALUATION BOARD

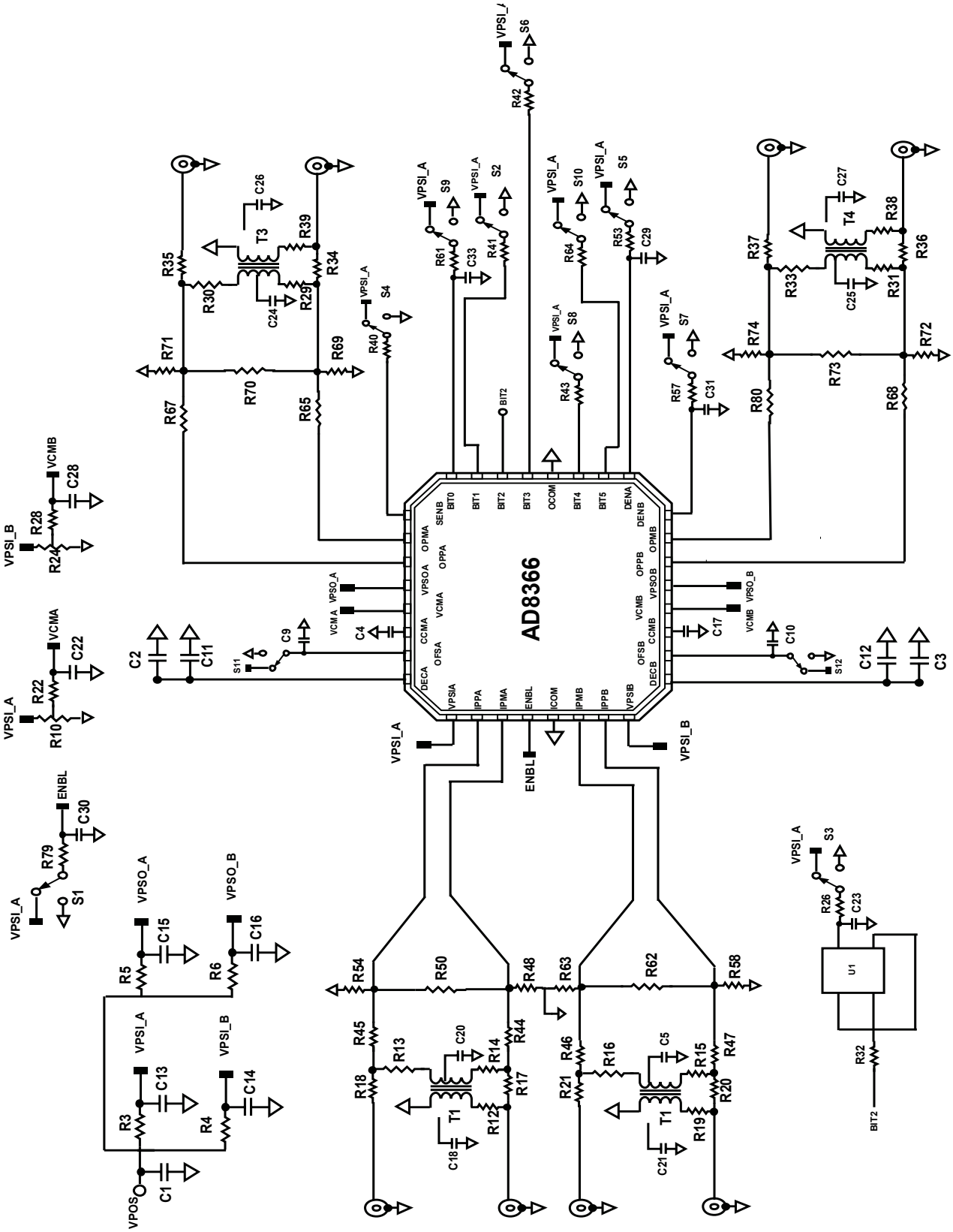

Figure 10. Evaluation Board Schematic

Table 4. Evaluation Board Configuration Options

Components	Function	Default Conditions
C1, C13 to C16, R3 to R6	**Power Supply Decoupling.** Nominal supply decoupling consists a 0.1µF capacitor to ground followed by 0.01 µF capacitors to ground positioned as close to the device as possible.	C1 = 0.1µF (size 0603) C13 to C16 = 0.01 µF (size 0402) R3 to R6 = 0 Ω (size 0603)
T1, T2, C5,C18,C20,C21, R12 to R21, R44 to R48, R50, R54, R58, R62, R63	**Input Interface.** The default configuration of the Eval board is for single ended operation. T1 and T2 are 4:1 impedance ratio baluns to transform a 50 Ω single-ended input into a 200 Ω-balanced differential signal. R12 to R14 and R15, R16, and R19 are populated for appropriate balun interface. R44 to R48 and R50, R54, R58, R62, andR63 are provided for generic placement of matching components. C5 to C20 are balun decoupling capacitors. R17, R18, R20, R21 can be populated with 0 Ω and the balun interfacing resistors can be removed to bypass T1 and T2 for differential interfacing.	T1, T2 = ADT4-6T+ (Mini-Circuits) C5,C20 = 0.1 µF (size 0402) C18,C21 = Do not install R12 to R16, R19, R44 to R47= 0 Ω (size 0402) R17, R18, R20, R21,R48, R50, R54, R58, R62, andR63 = open (size 0402)
T3, T4, C24 to C27, R29 to R31,R33 to R39,R65,R67 to R74, R80	**Output Interface.** The default configuration of the Eval board is for single ended operation. T3 and T4 are 4:1 impedance ratio baluns to transform a 50 Ω single-ended output into a 200 Ω-balanced differential load. R29 to R31, R33, R38, R39 are populated for appropriate balun interface. R65, R67 to R74, and R80 are provided for generic placement of matching components. C24, C25 are balun decoupling capacitors. R34 to R37 can be populated with 0 Ω and the balun interfacing resistors can be removed to bypass T3 and T4 for differential interfacing.	T3, T4 = ADT4-6T+ (Mini-Circuits) C24,C25 = 0.1 µF (size 0402) C26,C27 = Do not install R29 to R31, R33, R38, R39, R65, R67, R68, R80 = 0 Ω (size 0402) R34 to R37, R69 to R74= open (size 0402)
S1, S5, S7, R53, R57, R79, C29, C30, C31	**Enable Interface.** *-Device Enable.* The AD8366 is enabled by applying a logic high voltage to the ENBL pin. The device is enabled when the switch S1 is set in the down position (HIGH), connecting the ENBL pin to VPOS. *-Data Enable.* DENA and DENB are used to enable the data path for Channel A and Channel B respectively. Channel A is enabled when the switch S5 is set in the down position (HIGH), connecting the DENA pin to VPOS. Likewise, Channel B is enabled when the switch S7 is set in the down position (HIGH), connecting the DENB pin to VPOS. Both channels are disabled by setting the switches to the up position, connecting the DENA and DENB pins to GND.	S1,S5,S7 = installed R53, R57= 5.1kΩ (size 0603) R79 = 10kΩ (size 0402) C30=0.01uF (size 0402) C29, C31=1500pF (size 0402)
S2,S3,S4,S6,S8,S9, S10 R26, R32, R40-R43, R61,R64 C23, C33 U1	**Serial/Parallel Interface Control.** SENB is used to set the data control either in parallel or serial mode. Parallel Interface is enabled when the switch S4 is up position (LOW). Serial interface enabled when S4 is in the down position (HIGH). For SENB pulled LOW, BIT0 (switch S9) sets 0.25dB Gain BIT1 (switch S2) sets 0.5dB Gain BIT2 (switch S3) sets 1dB Gain BIT3 (switch S6)sets 2dB Gain BIT4 (switch S8)sets 4dB Gain BIT5 (switch S10) sets 8dB Gain For SENB pulled HIGH, BIT0 becomes a chip-select (CS), BIT1 becomes serial data input, SDAT, and BIT2 becomes serial clock, SCLK. BIT3-BIT5 are not used in the serial mode.	S2,S3,S4, S6, S8, S9, 10 = installed R26=698 kΩ (size 0603) R32, R40-R43, R61,R64 = 5.1kΩ (size 0603) C23, C33 = 1500pF (size 0603) U1= SN74LVC2G14, Clock Chip
S11, S12, C9, C10	**DC Offset Correction Loop Compensation.** The DC offset correction loop is enabled (HIGH) with switch S11 and S12 for channel A and channel B respectively. When enabled, the capacitor is connected to circuit common. When disabled (LOW), the OFSA/OFSB pins are tied to common.	S11, S12 = installed C9, C10=8200pF (size 0402)

R10, R22, R24, R28, C22, C28	**Output Common-mode Setpoint.** The output common mode on channels A and B can be set externally when applied to the VCMA and VCMB. The resistive change thorough the potentiometer sets a variable VCMA voltage. If left open, the output common mode defaults to Vpos/2.	R10, R24= 10 kΩ Potentiometers R22, R28= 0Ω
C2, C3, C11, C12	Vpos/2 Reference Output Decoupling Capacitor to circuit common.	C2, C3= 0.1µF (size 0402) C11, C12= 0.01µF (size 0402)
C4, C17	**Output Common-mode Centering Loop Compensation.** Connect capacitor to circuit common	C4, C17= 1 nF (size 0402)

PARALLEL AND SERIAL INTERFACE TIMING

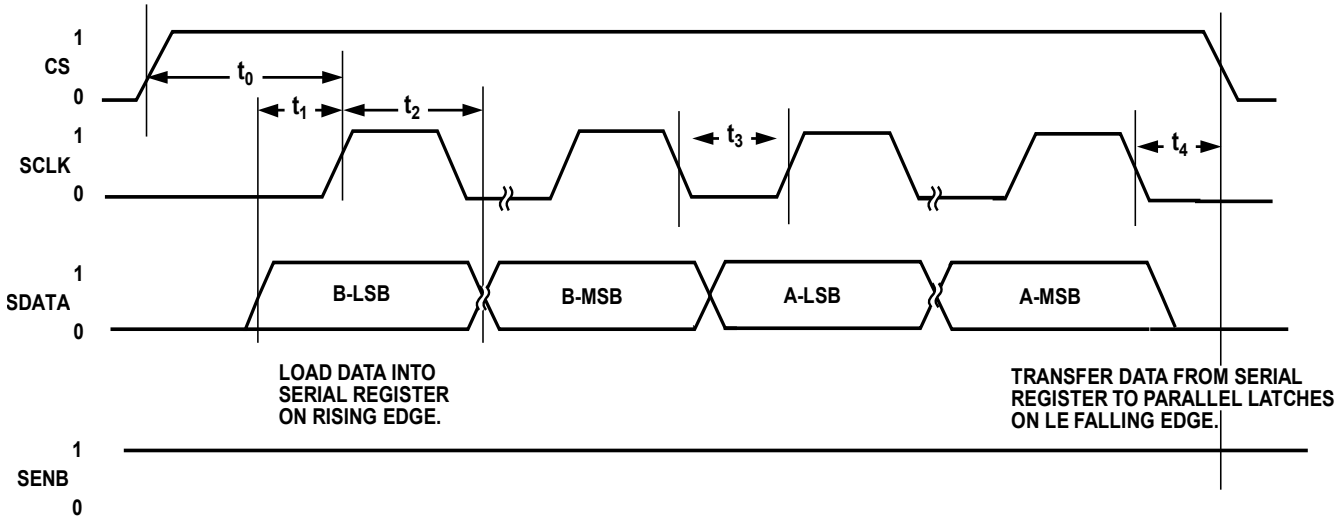

Figure 11. SPI Port Timing Diagram

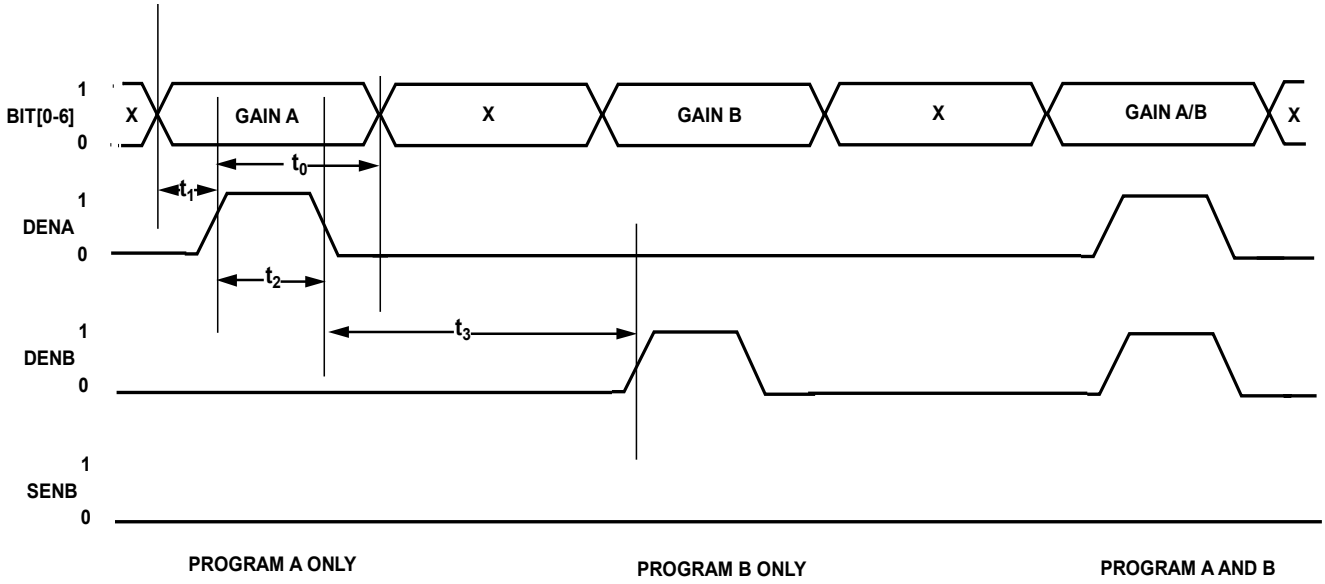

Figure 12. Parallel Port Timing Diagram

OUTLINE DIMENSIONS

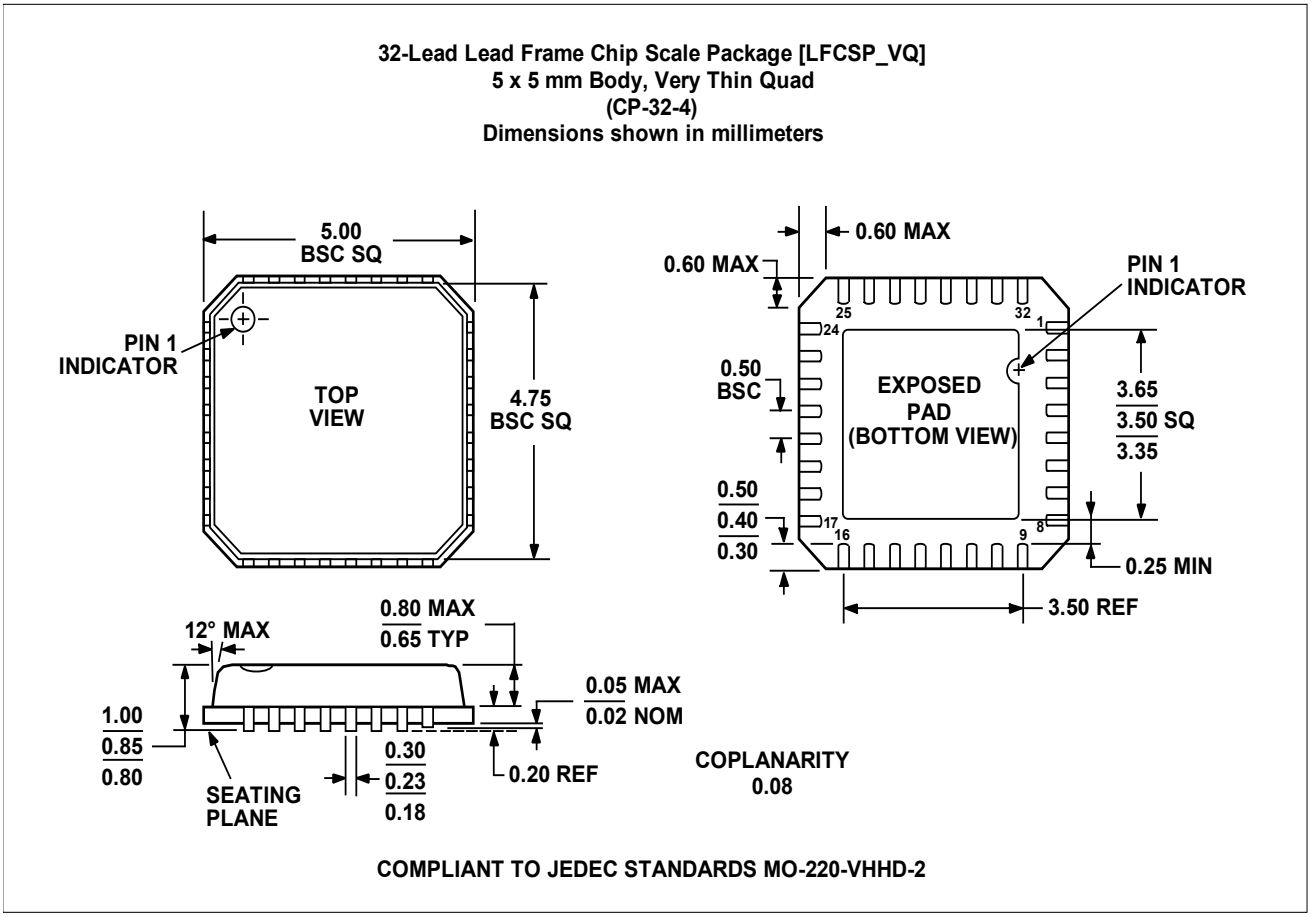

Figure 13. Outline Dimensions.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8366-EVALZ		Evaluation Board	